1. FEATURES

- 4-phase motors up to 10A coil current
- Voltage Range 13V to 60V DC ($65V_{abs}$ MAX)
- Gate Drive 1.0A Source 1.0A Sink
- Drives High−Side PMOS and Low−Side NMOS
- Inverting Channel B Biases High−Side PMOS Device Off when VDD is below UVLO Threshold
- TTL Input Thresholds
- Internal Resistors Turn Driver Off If No Inputs
- Electrostatic Discharge (ESD) Protected: 4kV
- -40°C to 125°C operating temperature range

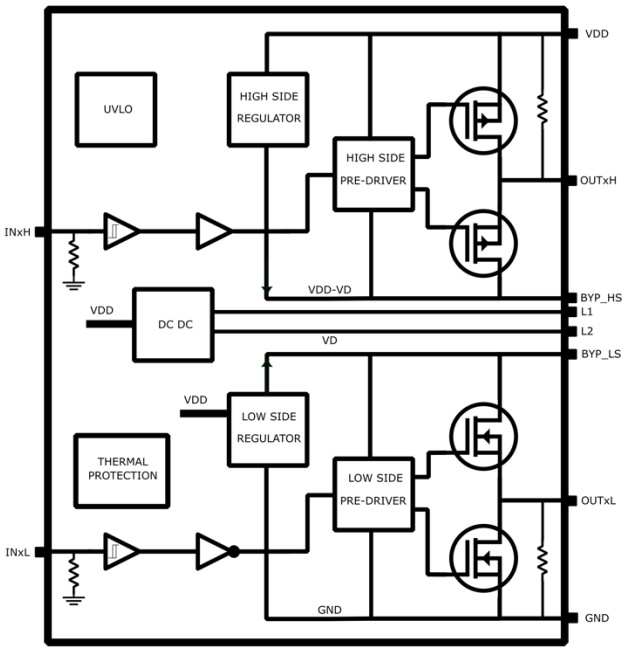
2. APPLICATIONS

3. DESCRIPTION

The VS6111GD is a 4x dual 1.0 A gate driver tailored to drive a high-side P-channel MOSFET and a low-side N-channel MOSFET in motor control applications operating with voltages up to 60V. With TTL input thresholds, it provides buffering and level translation from logic inputs. An internal under-voltage lockout feature disables the output switching devices if the VDD supply voltage falls below the required operating level. Built-in 100kΩ resistors ensure the non-inverting output is biased low, and the inverting output is biased to VDD, keeping the MOSFETs off during startup when logic control signals may be absent.

The VS6111GD's innovative final output stage architecture uses MOSFET output drivers, delivering high current during the MOSFET's Miller plateau phase to reduce switching losses, while ensuring a full rail-to-rail voltage swing and reverse current capability. If an input is left unconnected, internal resistors bias the inputs to keep the external MOSFETs off. Integrated DC-DC has 4.5V reference and it can be used to generate 4.5V or 5V DC voltages to supply current to external devices.

4. Block Diagram

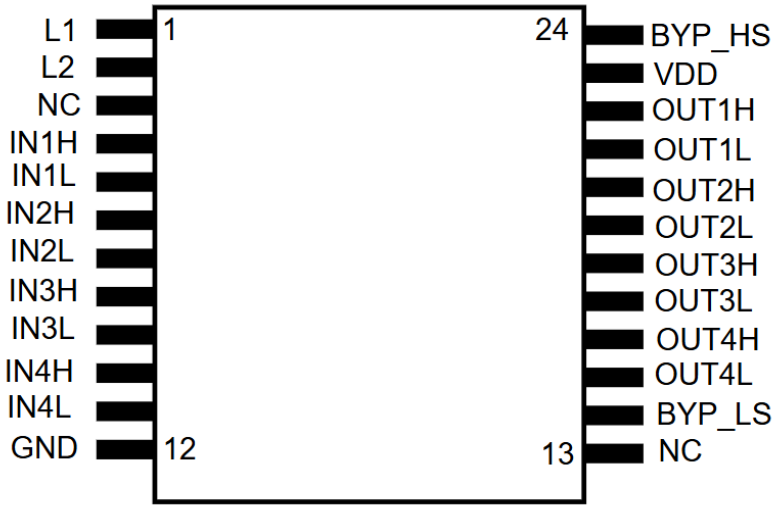


5. Device Variants

DEVICE NAME	NO OF CHANNELS	PACKAGE	TEMPERATURE
VS6111GD	4	SSOP24	-40°C to 125°C

6. CHIP PINOUT AND PACKAGE

PACKAGE TYPE SSOP 24PIN (PLASTIC SMALL OUTLINE)



3.9 mm×8.65 mm; Thickness,1.45mm; Pitch, 0.635 mm

7. PIN FUNCTIONALITY

Name	PIN	I/O	Function
L1	1	Inout	DC-DC Inductor pin 1
L2	2	Inout	DC-DC Inductor pin 2
NC	3	NC	Not Connected
IN1H	4	Input	High Side Control Input Channel 1
IN1L	5	Input	Low Side Control Input Channel 1
IN2H	6	Input	High Side Control Input Channel 2
IN2L	7	Input	Low Side Control Input Channel 2
IN3H	8	Input	High Side Control Input Channel 3
IN3L	9	Input	Low Side Control Input Channel 3
IN4H	10	Input	High Side Control Input Channel 4
IN4L	11	Input	Low Side Control Input Channel 4
GND	12	Supply	Ground
NC	13	NC	Not Connected
BYP_LS	14	Output	Low Side Gate driver supply output
OUT4L	15	Output	Low Side Output Channel 4
OUT4H	16	Output	High Side Output Channel 4
OUT3L	17	Output	Low Side Output Channel 3

OUT3H	18	Output	High Side Output Channel 3
OUT2L	19	Output	Low Side Output Channel 2
OUT2H	20	Output	High Side Output Channel 2
OUT1L	21	Output	Low Side Output Channel 1
OUT1H	22	Output	High Side Output Channel 1
VDD	23	Supply	Power Supply
BYP_HS	24	Output	High Side Gate driver supply output

8. ELECTRICAL SPECIFICATIONS

8.1 ABSOLUTE MAXIMUM RATINGS

PARAMETERS	I/O SIGNALS/POWER	MIN	MAX
Power Supply Voltage	VDD to GND	–0.3V	65 V
Input voltage	INx[H,L] to GND	GND – 0.3	DVDD + 0.3
Output voltage	OUTx[H,L] to GND	GND – 0.3	DVDD + 0.3
Temperature	Junction Temperature		150°C
Temperature	Storage Temperature	–60°C	150°C

NOTE: Exceeding the Absolute Maximum Ratings can result in permanent damage to the device. These ratings are intended only as stress limits and do not ensure functional operation of the device at these or any other conditions outside the Recommended Operating Conditions. Prolonged exposure to conditions at the absolute maximum ratings may compromise device reliability.

8.2 ESD RATINGS

Human-body model (HBM)	±4000V	
Charged-device model (CDM)	±1000V	
IEC 61000-4-2 (Contact)	TBD	
IEC 61000-4-2 (Air discharge)	TBD	
Latch-Up Immunity	TBD	

8.3 RECOMMENDED OPERATING CONDITIONS

PARAMETER	MIN	TYP	MAX
Power Supply (VDD-GND)	4.5V	40V	60V
Digital Input Voltage (DVDD-GND)	GND – 0.1		5.5 + 0.1
Operating Ambient Temperature	–40°C		125°C

8.4 ELECTRICAL CHARACTRISTICS

(Unless otherwise noted, VDD = 40 V and TJ = −40°C to +125°C. Currents are defined as positive into the device (Isink) and negative out of the device (Isource).

PARAMETER	MIN	Typical	MAX	UNITS
Optimum Operating Range	see UVLO	48	60	Volts
Supply Current Inputs	0.7	0.7	0.9	mA
Turn−On Voltage (VDD)	9.7	11.3	12.8	Volts
Turn−On / Turn−Off Hysteresis	400	650	1240	mV
Inx Logic Low Threshold	0.93	1.1	1.21	Volts
Inx Logic High Threshold	1.74	1.9	2	Volts
Logic Hysteresis Voltage		0.7		Volts
Input pulldown Resistance		100		KOhm
OUT Current, Peak, Turn−Off (CLOAD = 0.1 uF, f = 1 kHz)		2.5		A
OUT Current, Peak, Turn−On (CLOAD = 0.1 uF, f = 1 kHz)		-1.5		A
OUTL Drive Voltage (VDD = 60 V)	10.2	11	12.3	V
OUTH Drive Voltage (VDD = 60 V)	VDD-10.2	VDD-11.2	VDD-12.5	V
OUTL Drive Voltage (AFTER UVLO TRIGGER)	8	8.5	9.8	V
OUTH Drive Voltage (AFTER UVLO TRIGGER)	8.4	VDD-9.2	10.4	V
OUTL Sink Impedance (Turn−Off)	0.36	0.56	0.94	Ohm
OUTL Source Impedance (Turn−On)	1.14	1.6	2.49	Ohm
OUTH Sink Impedance (Turn−On)	0.29	0.45	0.75	Ohm
OUTH Source Impedance (Turn−Off)	0.68	0.95	1.49	Ohm
OUTL Rise Time (CLOAD = 1000 pF to GND)	8.2	9.1	14.1	ns
OUTL Fall Time (CLOAD = 1000 pF to GND)	4.7	5.5	7.9	ns
OUTH Rise Time (CLOAD = 1000 pF to VDD)	4.6	5.2	7	ns
OUTH Fall Time (CLOAD = 1000 pF to VDD)	5.5	6.1	8.6	ns
Output Propagation Delay On from IN to OUT (High side channel)	17.79	26.52	40.72	ns

Output Propagation Delay Off from IN to OUT (High side channel)	38.76	54.11	73.3	ns
Output Propagation Delay On from IN to OUT (Low side channel)	10.97	16.83	26.55	ns
Output Propagation Delay Off from IN to OUT (Low side channel)	22.95	44.07	32.45	ns
Output Reverse Current Withstand				A
Output switching frequency		100	200	kHz
Gate driver load LS		24		nC
Gate driver load HS		31		nC
Thermal Shutdown Temperature (TS)	135	142.5	150	Celsius
Thermal Shutdown Recovery		TS-5		Celsius
DC-DC Driver Output Voltage	4.41	4.95	5.62	Volt
DC-DC Efficiency @ 110 mA load	73.8	77.67	80.79	Percent
DC-DC Supply Current @110 mA load	12.29	14	15.7	mA

9. INPUT THRESHOLD

The VS6111GD driver features TTL input thresholds, enabling it to perform buffering and level translation for logic inputs. These thresholds adhere to standard TTL logic levels, remaining consistent regardless of the VDD voltage, and include a hysteresis voltage of around 0.7 V. This setup allows the inputs to accept a range of logic signal levels, where any voltage above 2 V is recognized as a logic HIGH. To ensure reliable performance, the driving signal for the TTL inputs should have fast rising and falling edges, with a slew rate of at least 6 V/µs. For example, a rise time from 0 to 3.3 V should be no more than 550 ns. If the slew rate is too slow, circuit noise may cause the driver input voltage to exceed the hysteresis level, potentially leading to unintended retriggering of the driver input.

10. STATIC SUPPLY CURRENT

The power loss in a chip encompasses standby power losses, LDO power losses, FET conduction and switching losses, and diode losses. The FET conduction loss dominates the total power dissipation within the chip. During startup and fault conditions, the output current exceeds the normal current; therefore, it's crucial to factor in these peak currents and their duration. The total device dissipation is the sum of the power dissipated in each of the three channels. The maximum power the device can dissipate depends on the ambient temperature and the effectiveness of heatsinking. Therefore, it's essential to consider these factors when designing the PCB and heatsinking.

11. GATE DRIVE CIRCUIT

VS6111GD incorporates internal regulators to regulate the gate drive voltage. The output pin slew rate is determined by this gate drive voltage and the load on the output. It is not user adjustable, but a series resistor can be added if a slower rise or fall time is needed at the MOSFET gate.

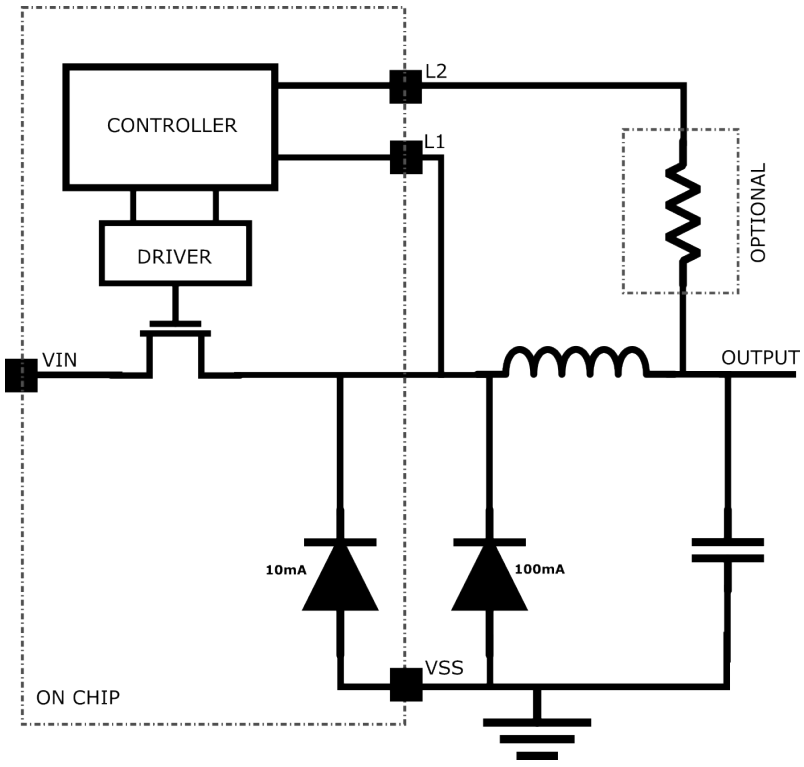
12. DC-DC CONVERTER

The VSGD611 features an integrated high-efficiency DC-DC converter that operates over a wide input voltage range of 13V to 60V, delivering a programmable output voltage from 4.5V to 10.0V with up to 110mA output current. Designed for flexibility, the output voltage can be easily adjusted using external resistors, making it suitable for different power supply requirements. The converter operates at variable switching frequency which is load dependent and highest upto 1.0MHz, ensuring compact external components and stable performance. Built-in protection features include under-voltage lockout (UVLO) and thermal shutdown at 150°C with automatic recovery at 130°C, ensuring reliable and safe operation across demanding conditions.

DC-DC converter operates with an external schottky diode if load current demand is less than 10mA but external diode is required if the current demand is more than 10mA at 60V supply.

Here is the equation for output voltage in case Roptional is used

Vout = 4.5*(Roptional+38K)/160K



13. STARTUP

13.1 UVLO CIRCUIT

If the voltage on the VDD pin drops below the VDD_UV threshold, all the integrated FETs, the DC-DC and the digital logic controller are disabled. Normal operation resumes (driver operation) once the undervoltage condition is removed. See the electrical specification for detail.

14. POWER SUPPLY REQUIREMENTS

14.1 Bulk De-Caps

In the design of motor drive systems, the appropriate local bulk capacitance is paramount. While higher capacitance generally offers benefits, it also entails increased costs and physical dimensions. The required local capacitance is influenced by various factors, including:

- The peak current demand of the motor system.
- The capacitance and current capability of the power supply.
- The parasitic inductance between the power supply and the motor system.
- The acceptable voltage ripple.
- The type of motor employed (brushed DC, brushless DC, stepper).
- The motor braking method.

The inductance between the power supply and the motor drive system restricts the rate of current change from the power supply. Insufficient local bulk capacitance may result in the system responding to excessive current demands or motor dumps by altering voltage. Conversely, adequate bulk capacitance ensures stable motor voltage and facilitates the rapid provision of high current. The minimal decoupling capacitor is 470nF.

15. LAYOUT GUIDELINES

The bulk capacitor should be positioned to minimize the distance of the high-current path through the motor driver device. To achieve this, the connecting metal trace widths should be as wide as possible, and numerous vias should be employed when connecting PCB layers. These practices reduce inductance, enabling the bulk capacitor to provide high current.

To minimize noise coupling and EMI interference from large transient currents into sensitive signal paths, separate grounding into GND and AGND. Vervesemi recommends connecting all non-power stage circuitry, to GND to reduce parasitic effects and enhance power dissipation.

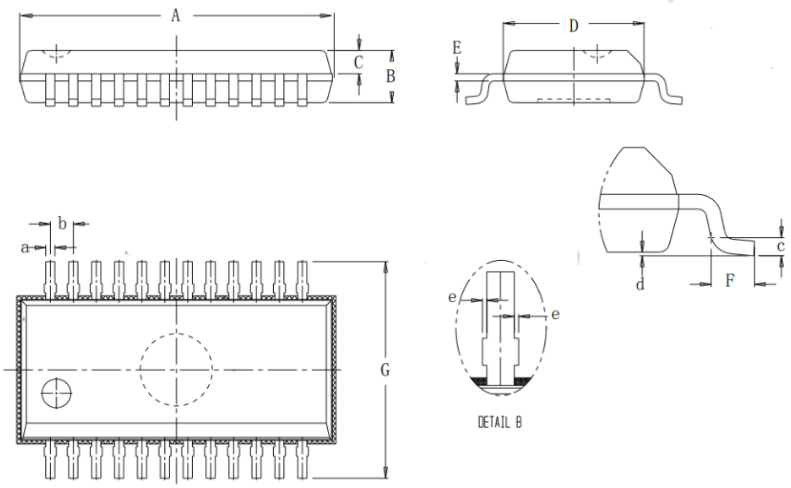
Ensure GND are connected using net-ties or wide resistors to minimize voltage offsets and maintain gate driver performance.

16. THERMAL GUIDELINES

The chip features a thermal shutdown (TSD) mechanism that disables the device if the die temperature exceeds a minimum of 130°C. Operation resumes once the temperature returns to a safe level.

Frequent thermal shutdown events indicate excessive power dissipation, inadequate heatsinking, or an excessively high ambient temperature.

17. PACKAGE DETAILS



COMMON DIMENSIONS

SYMBOL	MILLIMETER		
	MIN	MD	MAX
A	8.60	8.65	8.70
B	1.40	1.45	1.50
C	0.60	0.65	0.70
D	3.85	3.90	3.95
E	0.180	0.203	0.230
F	0.50	0.60	0.70
G	5.90	6.00	6.15
a	0.229	0.254	0.279
b	0.585	0.635	0.685
c		0.25	
d	0.00	0.05	0.10
e	–	–	0.10

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